In the embodiment illustrated in Figs. 1, 6, and 10-13, the poly-metal structure comprises a gate dielectric or other oxide layer 106, a polysilicon layer or region 108, a barrier layer 110, a metal layer 112, and a silicon dioxide layer 114. However, it is noted that a variety of additional poly-metal structures fall within the scope of the present invention. For example, referring to Fig. 14, the silicon dioxide layer 114 may be replaced by a layer 114' of $Si_3N_4$ or any other suitable material. Similarly, the barrier layer 110, which may comprise tungsten nitride, tungsten silicide, tungsten silicide nitride, titanium nitride, titanium silicide nitride, and combinations thereof may be replaced by one or more alternative layers or may be accompanied by additional layers of different materials.

Referring to Fig. 14, for example, the metal layer 112 may comprise tungsten and the barrier layer 110 may comprise tungsten nitride or tungsten silicide nitride. Alternatively, referring to Fig. 15, a titanium nitride layer 111 may be provided between the polysilicon layer 108 and a tungsten nitride layer 110. Referring to Figs. 16 and 17, it is noted that the metal layer 112 may comprise tungsten and the barrier layer may comprise a titanium nitride layer 111 or a titanium nitride layer 111 in combination with a titanium silicide nitride layer 113. Referring to Fig. 18, the poly-metal structure may be formed such that the metal layer 112 comprises tungsten and the barrier layer comprises tungsten silicide nitride 110 formed over tungsten silicide 109. Finally, referring to Fig. 19, it is noted that a barrier layer 110, e.g., tungsten nitride, may be interposed between a pair of metal layers 112, e.g., tungsten. In many instances, a tungsten nitride layer may be interposed between the tungsten layer 112 and the barrier layer 110.

Fig. 20 illustrates a top view layout of a memory device 100' including wordlines 104', digitlines 102', and a unit cell or memory cell 101'. The unit cell or memory cell 101' is one of many cells of the memory device 100'. The memory cell 101' illustrated in Fig. 20 has a feature size 105' in a first dimension that is half of the digitline pitch and a feature size 106' in a second dimension which matches the wordline pitch. It is noted that the present invention is not, however, limited to memory cells of a particular feature size. Nor is the present invention limited to particular wordline, digitline, or memory cell layout or geometry.

Fig. 21 is an illustration of a computer system 10 that can use and be used with embodiments of the present invention. The computer system 10 can be a desktop, network server, handheld computer or the like. As will be appreciated by those skilled in the art, the